## **CLAIMS**

What is claimed as new and desired to be protected by Letters Patent of the United States is:

1. An image pixel structure, comprising:

a semiconductor substrate of a first conductivity type having a surface;

a gate over a surface of the substrate; and

a photodiode within said substrate, said photodiode including an implant region of a second conductivity type, a portion of which extends further towards a region of said substrate beneath said gate than another portion of said implant region.

- 2. The image pixel structure of claim 1, wherein the substrate is p-type, and the implants are n-type.
- 3. The image pixel structure of claim 1, wherein the substrate is n-type, and the implants are p-type.
- 4. The image pixel structure of claim 1, wherein an upper portion of said implant region is farther away from the region beneath said gate than the other portions of the implant.

- 5. The image pixel structure of claim 1, wherein the implant region includes a first portion, said first portion being nearest the substrate surface in the implant region.
- 6. The image pixel structure of claim 5, wherein the implant dose of the first portion is between 2E11-1E13/cm<sup>2</sup>.
- 7. The image pixel structure of claim 5, wherein the implant region includes a second portion, said second portion being underneath the first portion in the implant region.
- 8. The image pixel structure of claim 7, wherein the implant dose of the second portion is between 2E11-1E13/cm<sup>2</sup>.
- 9. The image pixel structure of claim 7, wherein the implant region includes a third portion, said third portion being underneath the second portion in the implant region.
- 10. The image pixel structure of claim 9, where the implant dose of the third portion is between 2E11-1E13/cm<sup>2</sup>.
- 11. The image pixel structure of claim 9, wherein the first, second, and third portions of the implant region are formed by implants angled between 0 and 30 degrees in the direction of the gate, said angle being

measured away from a line normal to the surface of the substrate, with at least one of the implants being at an angle greater than 0 degrees.

- 12. The image pixel structure of claim 11, wherein the third portion extends further than the first and second portions towards the region of said substrate beneath said gate.
- 13. The image pixel structure of claim 9, wherein the implant angle for the first and second portions of the implant region is between 0-15 degrees, and the implant angle for the third portion is between 0-30 degrees, at least one of said implant angles being greater than 0 degrees.
- 14. The image pixel structure of claim 12, wherein the implant angle for the first and second portions of the implant region is between 0-10 degrees, and the implant angle for the third portion is between 0-15 degrees.
- 15. The image pixel structure of claim 11, wherein the second portion extends further than the first and third portions towards the region of said substrate beneath said gate.
- 16. The image pixel structure of claim 9, wherein the implant region includes a fourth portion, said fourth portion being lateral to the second portion in the direction of the gate.

- 17. The image pixel structure of claim 16, where the implant dose of the fourth portion is between 2E11-1E13/cm<sup>2</sup>.
- 18. The image pixel structure of claim 16, wherein the fourth portion extends further than the first, second, and third portions towards the region of said substrate beneath said gate.
- 19. The image pixel structure of claim 18, wherein the first, second, and third portions of the implant region are formed by implants angled between 0 and 5 degrees in the direction of the gate, said angle being measured away from a line normal to the surface of the substrate.
- 20. The image pixel structure of claim 19, wherein the fourth portion is formed by an implant angled between 10 and 30 degrees in the direction of the gate, said angle being measured away from a line normal to the surface of the substrate.
- 21. The image pixel structure of claim 1, wherein at least one of said portions of said implant region is angled.
- 22. The image pixel structure of claim 1, wherein the image pixel structure is a CCD imager.

- 23. The image pixel structure of claim 1, wherein the image pixel structure is a CMOS imager.
- 24. The image pixel structure of claim 23, wherein said image pixel structure is one of a three transistor (3T), four transistor (4T) five transistor (5T), six transistor (6T) and seven transistor (7T) structure.
- 25. The image pixel structure of claim 1, wherein said gate includes a gate oxide and a conductor.
- 26. The image pixel structure of claim 25, wherein said conductor contains at least one of poly-silicon, silicide, metal, and any combination of poly-silicon, silicide and metal.
- 27. The image pixel structure of claim 25, wherein said gate includes an insulator over the conductor.
- 28. The image pixel structure of claim 27, wherein the insulator is formed from at least one of oxide, nitride, metal oxide, and any combination of oxide, nitride, and metal oxide.
  - 29. A method of forming a region in an image sensor comprising:

    forming a semiconductor substrate of a first conductivity type
    having a surface;

forming a gate on the surface of the substrate; and

forming an implant region within said substrate of a second conductivity type, wherein a portion of said implant region extends further towards a region of said substrate beneath said gate, than another portion of said implant region.

- 30. The method according to claim 29, wherein the substrate is formed with p-type material, and the implants are formed by n-type materials.
- 31. The method according to claim 29, wherein the substrate is formed with n-type material, and the implants are formed by p-type materials.
- 32. The method according to claim 29, wherein an upper portion of said implant region is farther away from the region beneath said gate than the other portions of the implant.
- 33. The method of claim 29, wherein the forming of the implant region includes forming a first portion, said first portion being nearest the substrate surface in the implant region.
- 34. The method of claim 33, wherein the first portion is formed from an implant energy ranging between 5-200KeV.

- 35. The method of claim 33, wherein the forming of the implant region includes forming a second portion, said second portion being underneath the first portion in the implant region.
- 36. The method of claim 35, wherein the second portion is formed from an implant energy ranging between 30-200KeV.
- 37. The method of claim 35, wherein the forming of the implant region includes forming a third portion, said third portion being underneath the second portion in the implant region.
- 38. The method of claim 37, wherein the third portion is formed from an implant energy ranging between 60-300KeV.
- 39. The method of claim 37, wherein at least one of said first, second, and third portions of the implant region is formed by implants angled between 0 and 30 degrees in the direction of the gate, said angle being measured away from a line normal to the surface of the substrate, at least one of said portions having an implant angle greater than 0 degrees.
- 40. The method of claim 39, wherein the third portion extends further than the first and second portions towards the region of said substrate beneath said gate.

- 41. The method of claim 40, wherein the implant angle for the first and second portions of the implant region is 0-15 degrees, and the implant angle for the third portion is 0-30 degrees, wherein at least one of the first and second portions is angled greater than 0 degrees.
- 42. The method of claim 39, wherein the second portion extends further than the first and third portions towards the region of said substrate beneath said gate.
- 43. The method of claim 42, wherein the implant angles for the first, second and third portions of the implant region are 0-15 degrees, 0-30 degrees, and 0-30 degrees, respectively, wherein at least one of the implants is angled greater than 0 degrees.
- 44. The method of claim 37, wherein the forming of the implant region includes a fourth portion, said fourth portion being lateral to the second portion in the direction of the gate.
- 45. The method of claim 44, wherein the fourth portion is formed from an implant energy ranging between 50-150KeV.
- 46. The method of claim 44, wherein the fourth portion extends further than the first, second, and third portions towards the region of said substrate beneath said gate.

- 47. The method of claim 44, wherein at least one of said first, second, and third portions of the implant region are formed by implants angled between 0 and 10 degrees in the direction of the gate, said angle being measured away from a line normal to the surface of the substrate.
- 48. The method of claim 47, wherein the implant angle of the fourth portion is between 10 and 30 degrees.
- 49. The method of claim 35, wherein at least one of said first and second portions of implant region are formed by implants angled between 0-30 degrees in the direction of the gate, said angle being measured away from a line normal to the surface of the substrate.
- 50. The method of claim 29, wherein said gate includes a gate oxide and a conductor.
- 51. The method of claim 50, wherein said conductor contains at least one of poly-silicon, silicide, metal, and any combination of poly-silicon, silicide and metal.
- 52. The method of claim 29, wherein said gate includes an insulator over the conductor.

- 53. The image pixel structure of claim 52, wherein the insulator is formed from at least one of oxide, nitride, metal oxide, and any combination of oxide, nitride, and metal oxide.
  - 54. A pixel imager system, comprising:
    - (i) a processor; and
  - (ii) a CMOS imaging device coupled to said processor and including:

a pixel array, at least one pixel of said array comprising:

- a semiconductor substrate of a first conductivity type having a surface;
  - a gate over a surface of the substrate; and
- a photodiode, within said substrate, said photodiode including an implant region of a second conductivity type, a portion of said implant region which extends further towards a region of said substrate beneath said gate than another portion of said implant region.
- 55. The pixel imager system of claim 54, wherein the substrate is p-type, and the implants are n-type.

- 56. The pixel imager system of claim 54, wherein the substrate is n-type, and the implants are p-type.
- 57. The pixel imager system of claim 54, wherein an upper portion of said implant region is farther away from the region beneath said gate than the other portions of the implant.
- 58. The pixel imager system of claim 54, wherein the implant region includes a first portion, said first portion being nearest the substrate surface in the implant region.
- 59. The pixel imager system of claim 58, wherein the implant dose of the first portion is between 2E11-1E13/cm<sup>2</sup>.
- 60. The pixel imager system of claim 58, wherein the implant region includes a second portion, said second portion being underneath the first portion in the implant region.
- 61. The pixel imager system of claim 60, wherein the implant dose of the second portion is between 2E11-1E13/cm<sup>2</sup>.
- 62. The pixel imager system of claim 60, wherein the implant region includes a third portion, said third portion being underneath the second portion in the implant region.

- 63. The pixel imager system of claim 62, where the implant dose of the third portion is between 2E11-1E13/cm<sup>2</sup>.
- 64. The pixel imager system of claim 62, wherein the first, second, and third portions of the implant region are formed by implants angled between 0 and 30 degrees in the direction of the gate, said angle being measured away from a line normal to the surface of the substrate, with at least one of the implants being at an angle greater than 0 degrees.
- 65. The pixel imager system of claim 64, wherein the third portion extends further than the first and second portions towards the region of said substrate beneath said gate.
- 66. The pixel imager system of claim 62, wherein the implant angle for the first and second portions of the implant region is between 0-15 degrees, and the implant angle for the third portion is between 0-30 degrees, at least one of said implant angles being greater than 0 degrees.
- 67. The pixel imager system of claim 65, wherein the implant angle for the first and second portions of the implant region is between 0-10 degrees, and the implant angle for the third portion is between 0-15 degrees.

- 68. The pixel imager system of claim 64, wherein the second portion extends further than the first and third portions towards the region of said substrate beneath said gate.
- 69. The pixel imager system of claim 62, wherein the implant region includes a fourth portion, said fourth portion being lateral to the second portion in the direction of the gate.
- 70. The pixel imager system of claim 69, where the implant dose of the fourth portion is between 2E11-1E13/cm<sup>2</sup>.
- 71. The pixel imager system of claim 69, wherein the fourth portion extends further than the first, second, and third portions towards the region of said substrate beneath said gate.
- 72. The pixel imager system of claim 71, wherein the first, second, and third portions of the implant region are formed by implants angled between 0 and 5 degrees in the direction of the gate, said angle being measured away from a line normal to the surface of the substrate.
- 73. The pixel imager system of claim 72, wherein the fourth portion is formed by an implant angled between 10 and 30 degrees in the direction of the gate, said angle being measured away from a line normal to the surface of the substrate.

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74. The pixel imager system of claim 54, wherein at least one of said portion of implant regions are angled.

- 75. The pixel imager system of claim 54, wherein the pixel imager system is a CCD imager.
- 76. The pixel imager system of claim 54, wherein the pixel imager system is a CMOS imager.
- 77. The pixel imager system of claim 76, wherein said imager device is one of a three transistor (3T), four transistor (4T) five transistor (5T), six transistor (6T) or seven transistor (7T) architecture.